Frequency-Division Multiplexing With Graphene Active Electrodes for Neurosensor Applications

Jinyong Kim, *Graduate Student Member, IEEE*, Carly V. Fengel, Siyuan Yu, *Graduate Student Member, IEEE*, Ethan D. Minot, and Matthew L. Johnston, *Senior Member, IEEE*

***Abstract*—Multielectrode arrays are used broadly for neural recording, both *in vivo* and for *ex vivo* cultured neurons. In most cases, recording sites are passive electrodes wired to external read-out circuitry, and the number of wires is at least equal to the number of recording sites. We present an approach to break the conventional N-wire, N-electrode array architecture using graphene active electrodes, which allow signal upconversion at the recording site and sharing of each interface wire among multiple active electrodes using frequency-division multiplexing (FDM). The presented work includes the design and implementation of a frequency modulation and readout architecture using graphene FET electrodes, a custom integrated circuit (IC) analog front-end (AFE), and digital demodulation. The AFE was fabricated in 0.18 μm CMOS; electrical characterization and multi-channel FDM results are provided, including GFET-based signal modulation and IC/DSP demodulation. Long-term, this approach can simultaneously enable high signal count, high spatial resolution, and high temporal precision to infer functional interactions between neurons while markedly decreasing access wires.**

***Index Terms*—Neural-recording, multi-channel, frequency division multiplexing (FDM), graphene.**

I. Introduction

LARGE-SCALE neural recording systems are crucial for understanding brain function at the level of neuron-to-neuron interactions [1]. These measurements are increasingly supported by IC-based readout for density, scalability, and localized signal processing [2]–[8]. However, high-signal-count recordings of a dense network of neurons is challenging due to physical limits of wiring density, which in turn limit spatial resolution [9]–[11]. For conventional electrical neural recording interfaces, recording sites are passive electrodes wired to read-out circuitry, where the number of access wires equals the number of recording sites. This one-to-one relationship between recording sites and access wires is a major obstacle to obtaining high-density recordings from large areas of the brain.

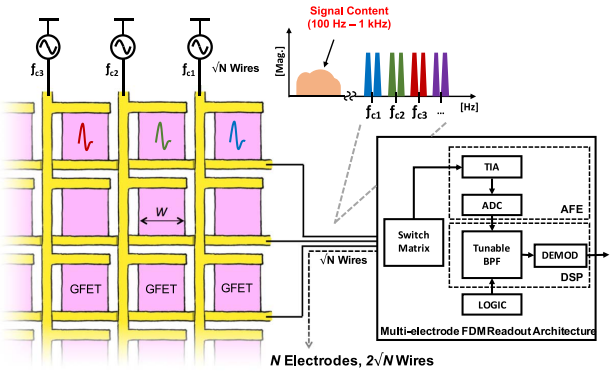

Fig. 1. Proposed high-level architecture using graphene field-effect transistor (GFET) active electrode array with FDM for access wire reduction.

A second bottleneck for large-scale neural recording is the signal conditioning and digitization electronics, which for highly-parallel recording systems are typically integrated in a microchip located outside the brain. For such implementations, the number of wires that can connect to an individual IC is physically limited, which has constrained state-of-the-art external neural interface ICs to typically less than 1000 sensor channels [3]–[5]. Internal neural interface ICs bonded to an electrode array [12], [13] can increase this density, but wire and packaging constraints may limit further scalability of such implementations. In some cases this can be addressed using IC-readout integrated into implantable electrode shanks [11], but for such approaches repeated relative micromotion between a rigid silicon probe and the surrounding brain tissue induces glial scarring and limits long-term use [14]. Electrode arrays that match the mechanical compliance of brain tissue and are stable in the biological environment have been demonstrated for both implantable [14] and brain surface [15] electrodes, but these material systems do not allow direct integration of electrical readout circuitry for wire reduction and still comprise passive, many-wire electrode arrays limited by wiring density.

In this brief, we propose and demonstrate proof-of-principle for the use of active graphene electrodes with a frequency-division multiplexing (FDM) architecture for use in neural

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Jinyong Kim, Siyuan Yu, and Matthew L. Johnston are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: kimjinyo@oregonstate.edu; yusiy@oregonstate.edu; matthew.johnston@oregonstate.edu).

Carly V. Fengel and Ethan D. Minot are with the Department of Physics, Oregon State University, Corvallis, OR 97331 USA (e-mail: fengelc@oregonstate.edu; ethan.minot@oregonstate.edu).

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recording and biosignal recording arrays. As illustrated in Fig. 1, each electrode is formed by a liquid-gated graphene field-effect transistor (GFET), which enables up-conversion of a local signal using a carrier frequency directly in the electrode. Using column-based FDM with shared-row readout, this GFET-FDM approach breaks the wire count limit of a conventional passive electrode array, without requiring the co-location of switches within the electrode array. In addition, the use of active GFET electrodes can enable flexible and compliant neural electrode arrays in future implementations.

II. Frequency-Division Multiplexing Approach Using Active Graphene Electrodes

A. Overview of the Approach

Compared to conventional passive electrodes, an active electrode provides gain or signal conditioning at the electrode itself. This can be accomplished for biological interfaces using fluid-gated FET devices, where the electrical resistance of the FET channel changes in response to local bioelectric signals, such as neuron firing [16]–[18]. Graphene, an atomically thin layer of sp^2 bonded carbon, can be used in this manner. A square of graphene has a baseline resistance on the order of 5 kΩ; this electrical resistance changes by approximately 1% when there is a local voltage change of 1 mV at the gate. Previous work has demonstrated that bioelectric signals of 10 μV can be detected with a 15 μm x 15 μm sensor size and 10 kHz bandwidth [17]. Moreover, graphene is ultra-flexible, mechanically robust, biocompatible, and chemically inert, which makes it a promising material for use in future flexible neural interface arrays.

A key insight of our proposed approach is that graphene FETs allows direct mixing of a local biosignal at the gate with a higher-frequency carrier signal applied to the source or drain, providing frequency-based modulation directly in each electrode. As illustrated in Fig. 1, this enables frequency-division multiplexing (FDM), where column-modulated output from multiple sensors is summed, sharing a single row wire for multiple graphene FET sensor signals. While demonstrated here using a few sensors as a proof of concept, the approach is broadly scalable for large, multi-electrode arrays.

B. Graphene Field-Effect Transistors

The basic structure of a graphene FET is shown in Fig. 2(a). A rectangle of CVD-grown graphene on an insulating glass substrate is contacted on either end by electrodes, forming source and drain connections. Electrodes are passivated using an insulating material (SU-8). A source-drain bias V_{sd} is applied across the graphene channel. A liquid electrolyte acts as the gate material, with a tungsten electrode applying a gate voltage V_g to the liquid and modulating the channel resistance. The electrolyte used for the data shown here is a combination of salts that closely replicate the salt concentrations in cell culture medium; the total salt concentration is 125 mM, with the main component being NaCl at a concentration of 116 mM.

The proof-of-principle device design used in this work is shown in Fig. 2(b). Two graphene FETs share a common drain electrode. Each FET has its own source electrode which can be driven by an ac voltage source at a unique frequency. The area of graphene exposed to the liquid gate is 20 μm x 50 μm.

To fabricate the 2-by-1 array of graphene FETs, a pattern for the metal electrodes was created using photolithography

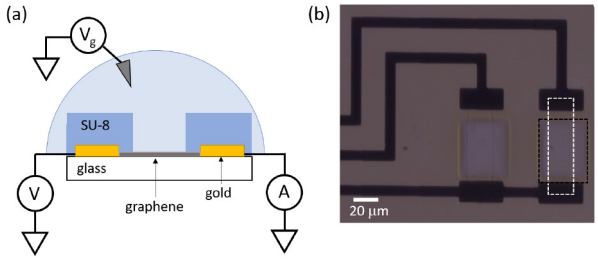

Fig. 2. Basic operation and design of a liquid-gated graphene FET: (a) Schematic of the cross-section of a graphene FET device. The gate is a liquid with a voltage applied by a tungsten probe. (b) A microscope image of two fabricated graphene FETs that share a common drain. The graphene is outlined in white and the SU-8 opening is outlined in black for the device on the right. The SU-8 insulates the gold source/drain leads from the electrolyte gate.

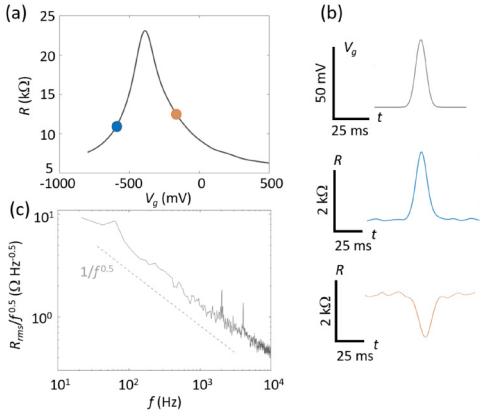

Fig. 3. Measured electronic properties of a graphene FET: (a) Device resistance as a function of the gate voltage. (b) The Gaussian pulse shown (top) was applied to the gate, and the resistance response (center and bottom) was recorded. The operating points (i.e., DC offset of the Gaussian pulse on V_g) are −550 mV for the blue curve, and −215 mV for the orange curve. When the offset is in a region with $dR/dV_g > 0$, such as at the blue point, the change in resistance is the same sign as the change in gate voltage. Conversely, when the offset is in the region $dR/dV_g < 0$, the change in resistance has the opposite sign as the gate voltage change. (c) The noise spectrum for the device shows a characteristic $1/f^{0.5}$ shape typical to graphene FETs. The spectrum was measured at $V_g = -215$ mV. The root-mean-square resistance R_{rms} at this operating point is ∼ 95 Ω for the range 100 Hz to 10 kHz.

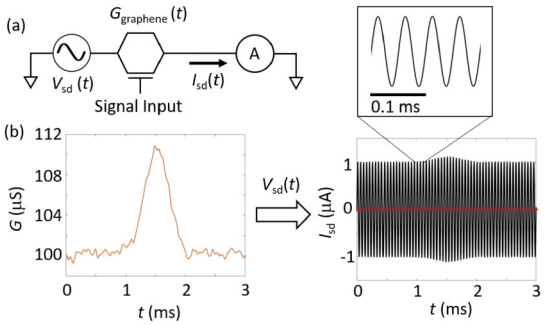

Fig. 4. Modulation of a signal by a graphene FET. (a) The circuit representation of the measurement system. (b) The conductance of the graphene FET (left) and the resultant modulated current (right).

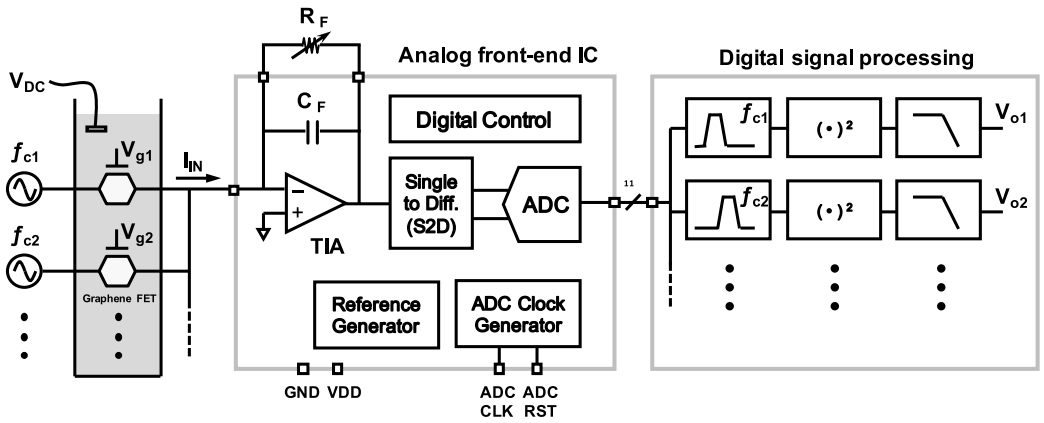

Fig. 5. Proposed system architecture using a graphene FET active electrode array for amplitude modulation and signal summing, with analog signal conditioning, digitization, and fully-digital square law demodulation used to demonstrate the scalable FDM approach using active electrodes.

on a glass substrate. The positive photoresist AZ 1512 (EMD Performance Materials) was spun onto the substrate, exposed, and developed with AZ 300 MIF developer. Next, approximately 10 nm of Cr followed by 60 nm of gold were deposited onto the chip with electron-beam deposition. The chip was soaked in Remover PG (MicroChem) overnight to remove the photoresist and excess metal. CVD-grown graphene (ACS Materials) was then placed onto the chip using a wet-transfer process. Photolithography and oxygen-plasma etch were used to pattern the graphene. Then a layer of SU-8 was spun on and patterned to form a protective layer over the metal leads. Windows of size 50 μm x 40 μm are opened above the graphene to allow for exposure to the electrolyte gate. After development, the SU-8 layer is approximately 1.5 μm thick. Electrical characterization of a typical graphene FET device is shown in Fig. 3.

Graphene sensors can perform amplitude modulation directly at the sensor site (Fig. 4). A change in gate voltage from a biological signal of interest (such as a neuron action potential) creates a change in the conductance, $G(t)$. The ac applied bias, $V_{sd}(t)$, is driven at a frequency f_c that is much faster than the biological signal of interest. The resulting ac current, $I_{sd}(t)$, has a carrier frequency f_c and is amplitude modulated by $G(t)$.

C. Analog Front-End Integrated Circuit Architecture

The basic signal architecture is shown in Fig. 5; signal modulation is performed in each graphene FET active electrode, and the summed FDM output is read out by a custom analog front-end (AFE) integrated circuit (IC) and demodulated using off-chip digital signal processing (DSP).

In the AFE, a transimpedance amplifier (TIA) converts the input current signal, which contains multiple modulated and combined signal channels from the graphene FET array, to a voltage signal. The feedback resistor R_F, which determines the gain of TIA, is externally placed for a flexible measurement setup; a feedback capacitor (C_F =500 fF) is added on-chip to improve stability. As R_F is not large (xx Ω), this can be included on-chip in future work without significant

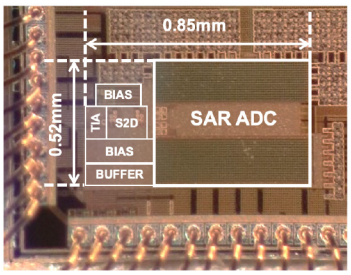

Fig. 6. Micrograph of the analog front-end IC fabricated in 0.18 μm CMOS.

area requirements. A folded-cascode amplifier structure is implemented as the op-amp with 75 dB open-loop gain and approximately 1.2 MHz unity gain bandwidth; gain must be flat across the range of modulation frequencies, although slight differences in per-channel gain (due to GFET or AFE) can be calibrated. At the output of the TIA, and single-ended to differential converter is used prior to the analog-to-digital converter (ADC) and also provides low-pass filter behavior for anti-aliasing.

An 11-bit successive-approximation register (SAR) ADC is implemented to digitize the modulated signal. Since the minimized unit capacitance of capacitor array can reduce the power consumption and increase the sampling speed, we chose a 7 fF standard finger metal-oxide-metal (FMOM) capacitor provided by the foundry, instead of a metal-insulator-metal (MIM) structure with a bigger minimum unit capacitance. As switching of the capacitor digital-to-analog converter (CDAC) in the SAR ADC is one of the critical points for power consumption, a merged capacitor switching technique [19] is implemented to reduce switching energy in this work.

The AFE IC was fabricated in 0.18 μm CMOS, and a die photo is shown in Fig. 6; the AFE occupies 0.44 mm^2.

D. Digital Signal Processing for Demodulation

For demodulation of the merged FDM signal, the back-end DSP chain contains a band-pass filter (BPF), a square operation block, and a low-pass filter (LPF). BPFs perform channel selection on the FDM waveform. Outputs of BPFs, each of

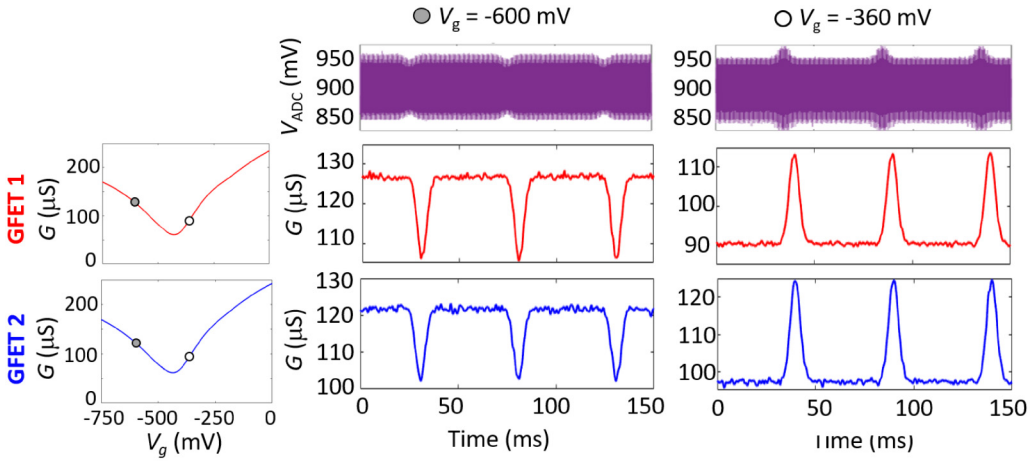

Fig. 7. Measured transient waveforms of two-channel GFET-modulated signals and demodulated signals at different DC gate bias voltages (V_g); a Gaussian pulse on GFET liquid gates mimics local neuron firing. Operation on either side of the Dirac point (−480 mV) yields negative and positive conductance change.

which contains only modulated signal content at a particular carrier frequency, are demodulated using square law demodulation. Namely, the signal is self-multiplied before it is filtered by LPF. Square-law demodulation is chosen because it does not require accurate phase information about the carrier waveform and is computational requirement is not high. In our envisioned system, the number of DSP chains equals to the number of carrier frequencies aggregated in the FDM waveform, such that simultaneous parallel demodulation of multiple sensor signals can be achieved.

The DSP architecture was first simulated in MATLAB and then implemented in verilog and synthesized for a commercial off-the-shelf FPGA module (Opal Kelly XEM6310) to provide real-time demodulation. As implemented, each BPF is a digital FIR filter with 48 taps and a nominal bandwidth of 2 kHz. The digital LPF uses 32 taps, with a cut-off frequency of 1 kHz. Squaring operation is performed on FPGA, whereas the final square root operation is done on the computer. The number of DSP chains and filter parameters are all reconfigurable based on the need of front-end circuitry. This FPGA-based digital back-end provides fast computation and high flexibility.

III. Experimental Results and Discussion

A. Experimental Setup

The experimental setup is shown in Fig. 8. Two graphene FETs with common drain (Fig. 2) were driven as described in Section II-B. A source-drain bias V_{sd} with frequency $f_{c1} = 5$ kHz was applied across device one, while V_{sd} with frequency $f_{c2} = 9$ kHz was applied across device two. The liquid gate was set to an operating point where device 1 and 2 are both sensitive to changes in gate voltage. A train of short voltage pulses, ΔV_g, was then added to the liquid gate to mimic a local bioelectric signal, such as a train of neuronal action potentials [17]. The total current was collected from the common drain. To achieve DC level-matching at the AFE IC input, an additional discrete amplifier, DC-blocking capacitor (0.9 μF), and series resistor (10 kΩ) were added at the AFE IC input (not shown in Fig. 5); these are not strictly required

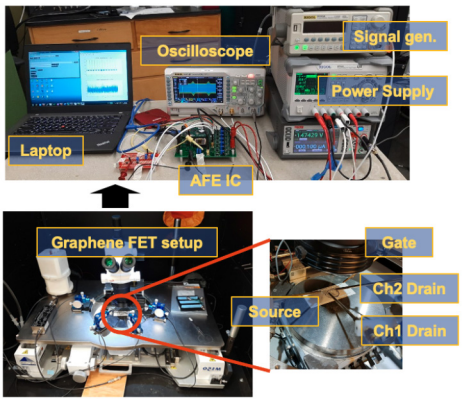

Fig. 8. Measurement setup for complete GFET-FDM architecture.

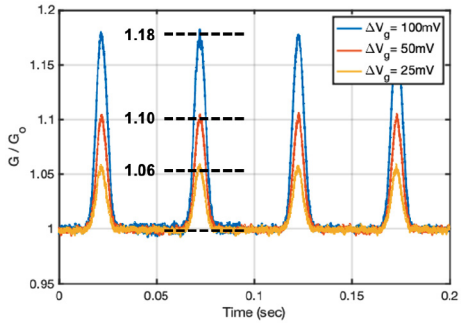

Fig. 9. Measured transient showing different amplitude of demodulated outputs at different gate voltage of graphene FET (ΔVg).

and are added to facilitate proof-of-concept while GFET devices are located on a probe station physically separate from the IC and PCB. In future, DC-coupled operation will be supported with correct DC level-matching. Data was either recorded at the ADC output (for subsequent digital signal processing using MATLAB, Fig. 7), or recorded at the output of the FPGA to demonstrate real-time DSP demodulation (Fig. 9).

B. Measured FDM Results From GFET-CMOS System

The top row of Fig. 7 shows the transient waveform recorded by the ADC, comprising the sum of 5 kHz and 9 kHz modulated signals from GFET 1 and GFET 2). The second and third rows show the demodulated output signals associated with GFET 1 and GFET 2 respectively. The experiment was performed at two different DC gate bias voltages. When $V_g = -600$ mV, dG/dV_g is negative, therefore, the sensor inverts the transient pulse ΔV_g. When $V_g = -360$ mV, dG/dV_g is positive and the sensor is non-inverting.

Fig. 9 shows 1-channel demodulated output as we vary the strength of the simulated signal, ΔV_g. When $\Delta V_g = 25$ mV, the conductance of the GFET is modulated by 6%. Extrapolating to the smaller ΔV_g, and comparing to the noise floor, we estimate that a modulation depth of 1% is detectable with our prototype design. This change in conductance would correspond to a 4 mV bioelectronic signal. While this demonstrates proof-of-concept for the GFET-FDM approach, further work is required to fully characterize and further minimize the noise floor of our system. By optimizing GFET fabrication and both AFE IC and DSP settings in future work, we anticipate that our FDM system can approach the 10 μV detection limit reported for direct measurements of a single GFET device [17].

IV. Conclusion

An FDM-based biosignal recording system was presented, which uses an array of graphene FET active electrodes for signal up-conversion directly at the sensor site. The architectural approach was validated using custom fabricated GFET devices, an AFE fabricated in 0.18 μm CMOS, and a digital back-end for signal demodulation. Experimental two-channel results demonstrate proof-of-concept for the GFET-FDM approach. This scalable architecture promises to enable significant wire count reduction for large-scale neural recording, and it partitions higher power sampling and demodulation functions to the back-end readout circuitry, where power is less constrained.

The use of atomically thin sensors is also promising for flexible substrates to provide dense, conformal neural sensor arrays for surface recordings. As an inherent tradeoff, maximum channel count be a function of input bandwidth, input dynamic range, modulation frequency, as well as of ADC sampling rate for this ADC-first approach. Future work will include increasing experimental channel count and *in vitro* testing with cultured neurons for biosignal validation. Long-term, this approach can support high-resolution active electrode arrays that simultaneously achieve high signal count, high spatial resolution, and sufficient temporal precision to infer functional interactions between neurons.

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